WHAT IS CLAIMED IS:

1. A process for estimating clock uncertainty between a receiving cell and a launching cell of a net, comprising steps of:

a) back-tracing a first path from the receiving cell toward a clock source and marking each cell having a predetermined characteristic along the first path;

b) back-tracing a second path from the launching cell toward the clock source to a predetermined marked cell; and

c) calculating clock uncertainty based on a delay associated with the first path between the marked cell and the receiving cell.

2. The process of claim 1, wherein the launching and receiving cells are data launching and receiving cells, the process includes:

identifying a first clock delay between the clock source and the launching cell,

identifying a second clock delay between the clock source and the receiving cell,

identifying a data delay between the launching cell and the receiving cell,

calculating a slack based on the first and second clock delays and the data delay, and

calculating clock uncertainty if the slack does not exceed a predetermined value.

3. The process of claim 2, further including:

calculating a common clock delay between the clock source and the predetermined marked cell, and

calculating clock uncertainty based on the second clock delay and the common clock delay.

4. The process of claim 3, wherein the clock uncertainty is a factor of a difference between the second clock delay and the common clock delay.

5. The process of claim 1, further including:

calculating a common clock delay between the clock source and the predetermined marked cell,

identifying a second clock delay between the clock source and the receiving cell, and

calculating clock uncertainty based on the second clock delay and the common clock delay.

6. The process of claim 1, wherein the launching and receiving cells are data launching and receiving cells and there are a plurality of data launching cells providing a plurality of data paths to one data receiving cell, the process comprising:

d) repeating steps b) and c) for each data launching cell to derive a clock uncertainty associated with each launching cell and the receiving cell, and

e) selecting the maximum value of clock uncertainty derived in step d) as a clock uncertainty for the receiving cell.

7. The process of claim 6, wherein the launching and receiving cells are data launching and receiving cells, the process further including:

identifying a first clock delay between the clock source and the launching cell,

identifying a second clock delay between the clock source and the receiving cell,

identifying a data delay between the launching cell and the receiving cell,

calculating a slack based on the first and second clock delays and the data delay, and

calculating clock uncertainty if the slack does not exceed a predetermined value.

8. The process of claim 7, further including:

calculating a common clock delay between the clock source and the predetermined marked cell, and

calculating clock uncertainty based on the second clock delay and the common clock delay.

9. The process of claim 6, further including:

calculating a common clock delay between the clock source and the predetermined marked cell,

identifying a second clock delay between the clock source and the receiving cell, and

calculating clock uncertainty based on the second clock delay and the common clock delay.

10. A process of optimizing a clock net in the form of a tree having a root defined by a driver pin and a plurality of leaves defined by driven pins, comprising steps of:

forcing a first buffer to a center of gravity of the plurality of leaves;

inserting a set of second buffers so each leaf is driven by an inserted buffer without timing violations; and

moving the first buffer to a center of gravity of the set of second buffers.

11. The process of claim 10, further including:

inserting a set of buffers to drive the second set of buffers without timing violations.

12. The process of claim 10, wherein the step of inserting a set of second buffers comprises:

selecting a subset of leaves driving by each second buffer based on a maximum load for the respective second buffer, and

connecting the respective second buffer to drive the selected subset of leaves.

13. The process of claim 10, further including estimating clock uncertainty based on a delay

associated with a path from the first buffer to each leaf.

14. The process of claim 13, further including:

identifying a second clock delay between the first buffer and each leaf, and

estimating clock uncertainty based on the maximum second clock delay.

15. A computer useable medium having a computer readable program embodied therein for addressing data to estimate clock uncertainty between a data receiving cell and a data launching cell of a net, the computer readable program comprising:

computer readable program code for causing the computer to back-trace a first path from the data receiving cell toward a clock source and mark each intermediate cell having a predetermined characteristic along the first path;

computer readable code for causing the computer to back-trace a second path from the data launching cell toward the clock source to a predetermined marked cell; and

computer readable code for causing the computer to calculate clock uncertainty based on a delay associated with the first path from the predetermined marked intermediate cell to the data receiving cell.

16. The computer useable medium of claim 15, wherein the launching and receiving cells are data launching and receiving cells, wherein the computer readable program includes:

computer readable code for causing the computer to identify a first clock delay between the clock source and the launching cell,

computer readable code for causing the computer to identify a second clock delay between the clock source and the receiving cell,

computer readable code for causing the computer to identify a data delay between the launching cell and the receiving cell,

computer readable code for causing the computer to calculate a slack based on the first and second clock delays and the data delay, and

computer readable code for causing the computer to calculate clock uncertainty if the slack does not exceed a predetermined value.

17. The computer useable medium of claim 16, further including:

computer readable code for causing the computer to calculate a common clock delay between the clock source and the predetermined marked cell, and

computer readable code for causing the computer to calculate clock uncertainty based on the second clock delay and the common clock delay.

18. The computer useable medium of claim 17, wherein the clock uncertainty is a factor of a difference between the second clock delay and the common clock delay.

19. The computer useable medium of claim 16, further including:

computer readable code for causing the computer to calculate a common clock delay between the clock source and the predetermined marked cell, and

computer readable code for causing the computer to identify a second clock delay between the clock source and the receiving cell, and

computer readable code for causing the computer to calculate clock uncertainty based on the second clock delay and the common clock delay.

20. The computer useable medium of claim 16, wherein the launching and receiving cells are data launching and receiving cells and there are a plurality of data launching cells providing a plurality of data paths to one data receiving cell, wherein the computer readable program includes:

computer readable code for causing the computer to repeat execution of the computer readable code that cause the computer to back-trace a second path and calculate clock uncertainty for each data launching cell to derive a clock uncertainty

associated with each launching cell and the receiving cell, and

computer readable code for causing the computer to select a maximum value of the derived clock uncertainties as a clock uncertainty for the receiving cell.